21 B Amdt
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicant	: Jigish D. Trivedi
Serial No.	: 08/915,658
Filed	: August 21, 1997
Title	: LOW RESISTANCE METAL SILICIDE LOCAL INTERCONNECTS
AND	METHOD OF MAKING
Docket	: MIO 0024 PA
Examiner	: G. Peralta
Art Unit	: 2814

Assistant Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on November 1, 2002

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AMENDMENT

This amendment is being filed in response to the Decision from the Board of Patent Appeals and Interferences mailed on October 4, 2002. A Request for Continued Examination accompanies this amendment. Reconsideration is respectfully requested in light of the amendments and remarks below.

CLEAN VERSION OF THE AMENDMENTS

A version of the amendments showing the markings is provided in a separate Appendix attached to this paper.

31. (Amended) A local interconnect comprising:

a composite structure comprising a first metal silicide, a second metal silicide and an intermetallic compound comprising metal from said first metal silicide and metal from said second metal silicide, wherein said intermetallic compound contains no non-metallic materials.

35. (Amended) A local interconnect for connecting a first active semiconductor region to a second active semiconductor region on a substrate assembly, said first and second active semiconductor regions being separated by an insulating region, said local interconnect comprising:

a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide, said refractory metal from said first refractory metal silicide being different from said refractory metal from said second refractor metal silicide, wherein said intermetallic compound contains no non-metallic materials.

37. (Amended) A semiconductor device comprising:

a substrate assembly having at least one semiconductor layer;

at least one field effect transistor formed in said at least one semiconductor layer, said least one field effect transistor having a source, a drain and a gate; and

a local interconnect for connecting at least one of said source, said drain and said gate to another active area within said substrate assembly, said local interconnect comprising a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide, wherein said intermetallic compound contains no non-metallic materials.

38. (Amended) A memory array comprising:

a plurality of memory cells arranged in rows and columns and formed on a substrate assembly having at least one semiconductor layer, each of said plurality of memory cells comprising at least one field effect transistor; and

at least one local interconnect for connecting at least one of a source, a drain and a gate of said at least one field effect transistor in one of said plurality of memory cells to one of an active area within said one memory cell or to one of a source, a drain and a gate of said at least one field effect transistor in another one of said plurality of memory cells, said local interconnect comprising a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide, wherein said intermetallic compound contains no non-metallic materials.